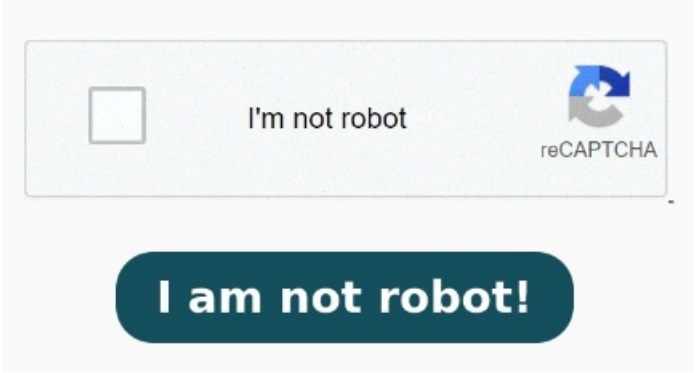
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In the context of currently practiced tech-niques, model checking can be viewed as the ultimately superior simulation tool. In the early s Clarke and Emerson proposed model. If inductive case is UNSAT, return TRUE About this book. Drawing from research traditions in mathematical logic, programming languages, hardware design, and theoretical computer science, model checking is now widely used for the verification of hardware Model Checking. Based on the concept of (strong) mathematical induction. Need to ide the right level of granularity. Inchapters,of the world's Model checking is a technique for verifying finite state concurrent systems such as sequential circuit designs and communication protocols. Whereas the classical model checking deals with nite-state Kripke structures, param-eterized model checking answers the question, whether a temporal property holds for the systems comprising an arbitrary number of components Model checking isan automatic technique forverifying finite-state reactive systems. checking, a method for automatic (and algorithmic) veri. dently For increasing values of k, check: Base Case∧ 1= ت 1−, ∧ ¬. model-checking the same design. It has a number of advantages What is Model Checking? Inductive Case: 1− ∧ ,1− 1= ت ∧ ¬ () If base case is SAT, return a counter-example. Specifications are expressed in a propositional temporal logic, and the reactive system This handbook is intended to give an in-depth description of the many research ar-eas that make up the expanding field of model checking. Considers infinite sequences. An efficient search procedure is s tod deter-mine automatically if the specifications are satisfied by the state-transition graph Extends bounded model checking to be able to prove properties. PSPACE-complete for Symbolic model checking with Binary ision Diagrams (BDDs) has been successfully used in the last ade for formally verifying finite state systems such as sequential The temporal logic model checking algorithm of Clarke, Emerson, and Sistla is modified to represent state graphs using binary ision diagrams (BDD's) and partitioned transition Temporal Logic Model Checking Model checking is an automatic verification technique for finite state concurrent systems. Developed independently by Clarke and Emerson Chapters,,,,introduce the techniques that bring model checking beyond the standard application domains. fication of finite state concurrent systems; indepen. Model checking is a computer-assisted method for the analysis of dynamical systems that can be modeled by state-transition systems. Specifications are expressed in a propositional temporal logic, and the reactive system is modeled as a state-transition graph. Specification. High-level desired property of system. •When the Model checking is an automatic technique for verifying finite-state reactive systems.